Listing of Claims

1. (Previously presented) A method of forming a capacitor on an integrated circuit comprising:

forming a cylindrical lower electrode of the capacitor on an integrated circuit substrate;

forming a nitride protection layer on the cylindrical lower electrode at a temperature below a minimum temperature associated with a phase change of the cylindrical lower electrode;

forming a dielectric layer on the nitride protection layer at a temperature of about 600°C or less, wherein the nitride protection layer is configured to limit oxidation of the cylindrical lower electrode during forming of the dielectric layer and wherein the nitride protection layer and the cylindrical lower electrode are not exposed to a temperature of above 600°C before formation of the dielectric layer; and

forming an upper electrode of the capacitor on the dielectric layer.

2. (Previously presented) The method of Claim 1 wherein the cylindrical lower electrode comprises an amorphous silicon layer, a polycrystalline silicon layer and/or a composite layer thereof.

3. (Previously presented) The method of Claim 1 wherein the nitride protection layer comprises a silicon nitride layer.

4. (Previously presented) The method of Claim 3 wherein forming the nitride protection layer comprises forming the silicon nitride layer at a temperature of about 600°C or less using a plasma nitration process.

5. (Previously presented) The method of Claim 3 wherein forming the nitride protection layer comprises forming the silicon nitride layer directly on the cylindrical lower electrode at a temperature of about 600°C or less using a chemical vapor deposition process

and/or an atomic layer deposition process.

6. (Previously presented) The method of Claim 3 wherein forming the nitride protection layer comprises forming the silicon nitride layer at a temperature of about 600°C or less using a microwave-type deposition process.

7. (Original) The method of Claim 1 wherein the dielectric layer comprises a metal oxide layer.

8. (Original) The method of Claim 7 wherein the metal oxide layer comprises a TiO_2 layer, an Al_2O_3 layer, an Y_2O_3 layer, a ZrO_2 layer, an HfO_2 layer, a $BaTiO_3$ layer, an $SrTiO_3$ layer and/or a composite layer thereof.

9. (Original) The method of Claim 7 wherein forming the dielectric layer comprises forming the metal oxide layer at a temperature of about 600°C or less using a chemical vapor deposition process and/or an atomic layer deposition process.

10. (Canceled).

11. (Original) The method of Claim 1 wherein the upper electrode comprises an amorphous silicon layer, a polycrystalline silicon layer, an Ru layer, a Pt layer, an Ir layer, a TiN layer, a TaN layer, a WN layer and/or a composite layer thereof.

12. (Previously presented) The method of Claim 1 wherein forming the cylindrical lower electrode comprises:

forming a lower structure on the integrated circuit substrate;

forming an insulation layer pattern having a contact hole on the lower structure;

forming a conductive plug in the contact hole;

forming an oxide layer patterned to have a cylindrical shape on the insulation layer

pattern and the conductive plug;

forming a conductive layer for the cylindrical lower electrode on the oxide layer; and removing the oxide layer to form the cylindrical lower electrode.

13. (Previously presented) The method of Claim 12 wherein forming the nitride protection layer comprises forming the nitride protection layer on the conductive layer.

14. (Previously presented) A method of forming a capacitor comprising:

forming a first conductive layer on a substrate;

forming a reaction-preventing nitride layer on the first conductive layer at a temperature not generating a phase change of the first conductive layer to prevent oxidation of the first conductive layer;

forming a dielectric layer on the reaction-preventing nitride layer at the temperature not generating the phase change of the first conductive layer, wherein the reaction-preventing nitride layer and the first conductive layer are not exposed to a temperature generating the phase change of the first conductive layer before formation of the dielectric layer; and

forming a second conductive layer on the dielectric layer.

15. (Original) The method of Claim 14 wherein the first conductive layer is an amorphous silicon layer, a polycrystalline silicon layer or a composite layer thereof.

16. (Previously presented) The method of Claim 14 wherein the reaction-preventing nitride layer is a silicon nitride layer.

17. (Previously presented) The method of Claim 16 wherein the silicon nitride layer is formed by a plasma nitration process at a temperature of about 600°C or less.

18. (Previously presented) The method of Claim 16 wherein the silicon nitride layer is formed by a chemical vapor deposition process at a temperature of about 600°C or

less or an atomic layer deposition process at a temperature of about 600°C or less.

19. (Previously presented) The method of Claim 16 wherein the silicon nitride layer is formed by a microwave-type deposition process at a temperature of about 600°C or less.

20. (Original) The method of Claim 14, wherein the dielectric layer is a metal oxide layer.

21. (Original) The method of Claim 20 wherein the metal oxide layer is at least one selected from the group consisting of a TiO_2 layer, an Al_2O_3 layer, an Y_2O_3 layer, a ZrO_2 layer, an HfO_2 layer, a $BaTiO_3$ layer, an $SrTiO_3$ layer and a composite layer thereof.

22. (Original) The method of Claim 20 wherein the metal oxide layer is formed by a chemical vapor deposition method at a temperature of about 600°C or less or by an atomic layer deposition method at a temperature of about 600°C or less.

23. (Original) The method of Claim 14 wherein the second conductive layer is an amorphous silicon layer, a polycrystalline silicon layer, a Ru layer, a Pt layer, an Ir layer, a TiN layer, a TaN layer, a WN layer and a composite layer thereof.

24. (Previously presented) A method of forming a capacitor comprising:

forming an insulation layer pattern having a contact hole on a substrate having a lower structure;

forming a first conductive layer continuously on a sidewall portion and a bottom portion of the contact hole and on the surface of the insulation layer pattern;

removing the first conductive layer formed on the surface of the insulation layer pattern;

removing the insulation layer pattern to allow the first conductive layer to remain on

the sidewall portion and the bottom portion of the contact hole to form a cylindrical lower electrode;

forming a reaction-preventing nitride layer on the cylindrical lower electrode at a temperature not generating a phase change of the cylindrical lower electrode to prevent oxidation of the cylindrical lower electrode;

forming a dielectric layer on the reaction preventing nitride layer at the temperature not generating the phase change of the first conductive layer, wherein the reaction-preventing nitride layer and the first conductive layer are not exposed to a temperature generating the phase change of the first conductive layer before formation of the dielectric layer; and

forming a second conductive layer on the dielectric layer as an upper electrode.

25. (Previously presented) The method of Claim 24 wherein the first conductive layer is an amorphous silicon layer, a polycrystalline silicon layer or a composite layer thereof.

26. (Previously presented) The method of Claim 24 wherein the reaction preventing layer is formed by a plasma nitration process at a temperature of about 600°C or less, a chemical vapor deposition process at a temperature of about 600°C or less or an atomic layer deposition process at a temperature of about 600°C or less.

27. (Previously Presented) The method of Claim 24 wherein the dielectric layer is at least one selected from the group consisting of a TiO_2 layer, an Al_2O_3 layer, an Y_2O_3 layer, a ZrO_2 layer, an HfO_2 layer, a $BaTiO_3$ layer, an $SrTiO_3$ layer and a composite layer thereof.

28. (Previously presented) The method of Claim 24 wherein the dielectric layer is formed by a chemical vapor deposition process at a temperature of about 600°C or less or by an atomic layer deposition process at a temperature of about 600°C or less.

29. (Original) The method of Claim 24 wherein the second conductive layer is one

of an amorphous silicon layer, a polycrystalline silicon layer, an Ru layer, a Pt layer, an Ir layer, a TiN layer, a TaN layer, a WN layer and a composite layer thereof.

30. (Previously presented) The method of Claim 24 wherein the lower structure includes a contact plug connected to the cylindrical lower electrode.

31. (Previously presented) The method of Claim 1 wherein the nitride protection layer comprises an electrically non-conductive layer.

32. (Previously presented) A method of forming a capacitor on an integrated circuit comprising:

forming a cylindrical lower electrode of the capacitor on an integrated circuit substrate;

forming an electrically non-conductive protection layer on the cylindrical lower electrode at a temperature below a minimum temperature associated with a phase change of the cylindrical lower electrode;

forming a dielectric layer on the electrically non-conductive protection layer at the temperature below the minimum temperature associated with the phase change of the cylindrical lower electrode, wherein the electrically non-conductive protection layer is configured to limit oxidation of the cylindrical lower electrode during forming of the dielectric layer and wherein the electrically non-conductive protection layer and the cylindrical lower electrode are not exposed to the temperature associated with the phase change of the cylindrical lower electrode before formation of the dielectric layer; and

forming an upper electrode of the capacitor on the dielectric layer.

33. (Previously presented) A method of forming a capacitor on an integrated circuit comprising:

forming a lower electrode of the capacitor on an integrated circuit substrate;

forming a nitride protection layer on the lower electrode at a temperature below a

minimum temperature associated with a phase change of the lower electrode;

forming a dielectric layer on the nitride protection layer at the temperature below the minimum temperature associated with the phase change of the lower electrode, wherein the nitride protection layer is configured to limit oxidation of the lower electrode during forming of the dielectric layer and wherein the nitride protection layer and the lower electrode are not exposed to the temperature associated with the phase change of the lower electrode before formation of the dielectric layer; and

forming an upper electrode of the capacitor on the dielectric layer.